REMARKS

This Amendment is responsive to the Office Action mailed October 20, 2004. Applicants acknowledge the allowability of claims 2 - 10 and 12 - 14 if rewritten in accordance with the requirements of the Office Action.

Claim Objections

Claims 6, 10, and 12 - 14 are objected to because the "alternate test" and the "signature test" do not appear to be properly defined in the specification, and because the word "rest" in claim 14 should be "retested." Claim 14 has been amended.

Applicant respectfully traverses the objections insofar as they are based on a perceived lack of definition of the terms "signature test" and "alternate test."

The meanings of these terms are provided in the "Background of the Invention" portion of the disclosure, on Page 2, as follows:

> Various alternate tests have been proposed to test products such as analog, mixed-signal and radio frequency electronic circuits in less time than is required by specification testing while minimizing any loss in yield of acceptable products compared to specification testing. Such tests are described in United States patent application Serial No. 09/575,488 entitled METHOD FOR TESTING CIRCUITS, hereby incorporated by reference in its entirety, and in United States patent application Serial No. 09/837,887 entitled METHOD AND APPARATUS FOR LOW COST SIGNATURE TESTING FOR ANALOG AND RF CIRCUITS, also hereby incorporated by reference in its entirety. In particular, it has been shown that if a carefully designed analog transient stimulus is applied to a DUT one or more of the DUT specifications can be mathematically extracted from the corresponding test response. Moreover, while the stimulus may be essentially continuous, such as a modulated waveform, it may also be simple and of short duration, resulting in a significant test-time reduction compared to specification test time. This form of testing is known as "implicit specification testing" or "signature testing."

The last sentence indicates that the term "signature testing" is a term of art having a known meaning to persons of ordinary skill in the art. As such, there is no need or requirement to define this term.

The term "alternate test" is described as referring to any number of tests that differ from "specification testing." Specification testing is discussed as follows, at Page 1:

> In the manufacture of products, particularly electronic semiconductor integrated circuit devices ("ICs") and electronic system-on-a-chip devices ("SOCs"), there often is conflict between adequately testing the products to ensure that they meet performance expectations, on the one hand, and minimizing manufacturing costs while maximizing product yield, on the other hand. Although quality control typically is enforced at various stages of the manufacturing process, the most effective way of identifying a defective device is to employ a final performance test, in which a sequence of test steps is applied to the device under test ("DUT"), each producing a value for a parameter of the device specifications. The DUT is considered to be acceptable or defective, that is, to pass or fail the test, based on whether the test values fall within a predetermined range of satisfactory parameter values established for the device specifications. This form of testing is referred to as "specification testing" and the individual tests are referred to as "production tests."

The disclosure here indicates that "specification testing" is also a term of art having a known meaning to persons of ordinary skill in the art. Taking the two paragraphs together, "alternate tests" are tests that differ from "specification testing" but that may include "signature testing." Since persons of ordinary skill know what "specification testing" and "signature testing" are, such persons will understand from the above paragraphs that an "alternate test" can be any species (or subset) of test strategies within a genus (or set) that excludes "specification test" but includes "signature test."

It should also be noted that the preamble to claim 1 further defines what is meant by "alternate test," i.e., that it "test[s] products with at most substantially the same margin of error as a specification test."

Section 103 Rejections

Claims 1, 11, and 15 - 19 stand rejected under 35 USC §103(a) as being unpatentable over Chatterjee et al., U.S. Patent No. 6,625,785 ("Chatterjee"). The Office Action acknowledges that Chatterjee qualifies only as prior art under 35 USC §102(e), so that 35 USC §103(c) applies. Applicants respectfully traverse the rejections.

Applicants do not concede that Chatterjee is prior art, and reserve their right to demonstrate that it is not, or that 35 USC §103(c) applies, if that should become necessary or desirable at some future time, but believe that the reference is inapposite, so that such showings should not become necessary.

Brief Description of Relevant Portions of Chatterjee

At Col. 3, line 59 - Col. 4, line 18, Chatterjee explains that the result of prior art performance testing is not good enough to determine how the manufacturing process should be tuned to improve yield. This is because it is too difficult to relate the performance measurements (or metrics) to manufacturing process parameters.

The invention is based on the recognition that the performance measurements can be related to device parameters, where it is known that the device parameters can be related to manufacturing process parameters, for tuning the manufacturing process.

Referring generally to Col. 4, line 56 - Col. 5, line 7, Chatterjee begins with original performance measurements, and then explains that an analysis is performed to determine whether device parameters can be computed therefrom. If that is not possible, optimized test stimuli are generated for producing optimized test responses from the device, to allow unique identification of the device parameters. Non-linear regression models relate the original performance measurements and the optimized test responses to device parameters. These models are used in "post-test" processing to solve for the device parameters. To diagnose yield problems, the contribution of each device parameter to variations in measured performance is identified by

decomposing the regression model into individual components pertaining to each device parameter and pertaining to interaction between device parameters.

Comparison of The Method of Chatterjee with that of the Rejected Claims

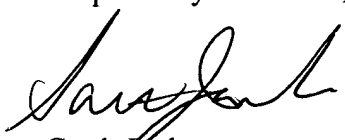
Claim 1 of the present invention presents a novel testing strategy for determining whether to accept or reject a product. It defines a specification test limit corresponding to a specification test but initially tests the product using an alternate test. If the product tests within an inner test error bound for the alternate test, it is accepted; if the product tests outside an outer test error bound for the alternate test it is rejected; and if the product test results fall in-between, it is retested using the specification test.

Chatterjee is different. A product is accepted or rejected based on standard IC testing. In the standard testing described, a gross test is used first to determine if the entire wafer is "good" or "bad." If the wafer tests "good," then performance testing is performed on individual IC's. An individual IC will either fall outside specification limits, in which case it will be rejected, or it will fall inside specification limits, in which case it will be accepted.

Chatterjee may perform additional testing, but it does not depend on whether the individual IC's test good or bad, and it is not used to decide whether to accept or reject them; rather, it is used to estimate device parameters and correlate the results with manufacturing process parameters so that the manufacturing process can be tuned to improve yield. None of this has anything to do with what is claimed in the present application.

Accordingly, it is respectfully submitted that the claims as amended are in condition for allowance, and the Examiner is respectfully requested to allow all of the claims and pass the case to issue.

Respectfully submitted,



Garth Janke
Reg. No. 40,662
(503)228-1841